*Fig.1*

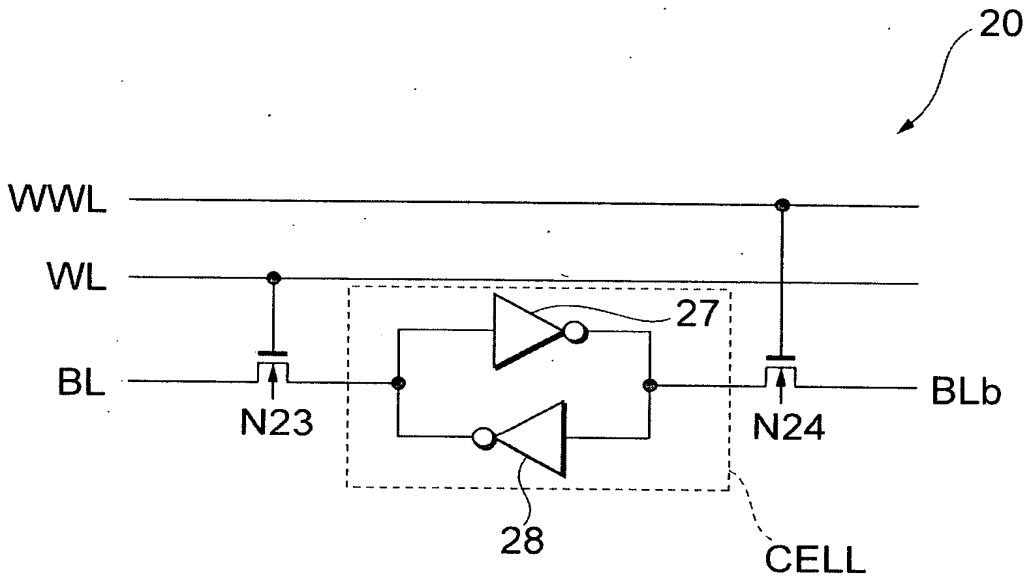


Fig. 2

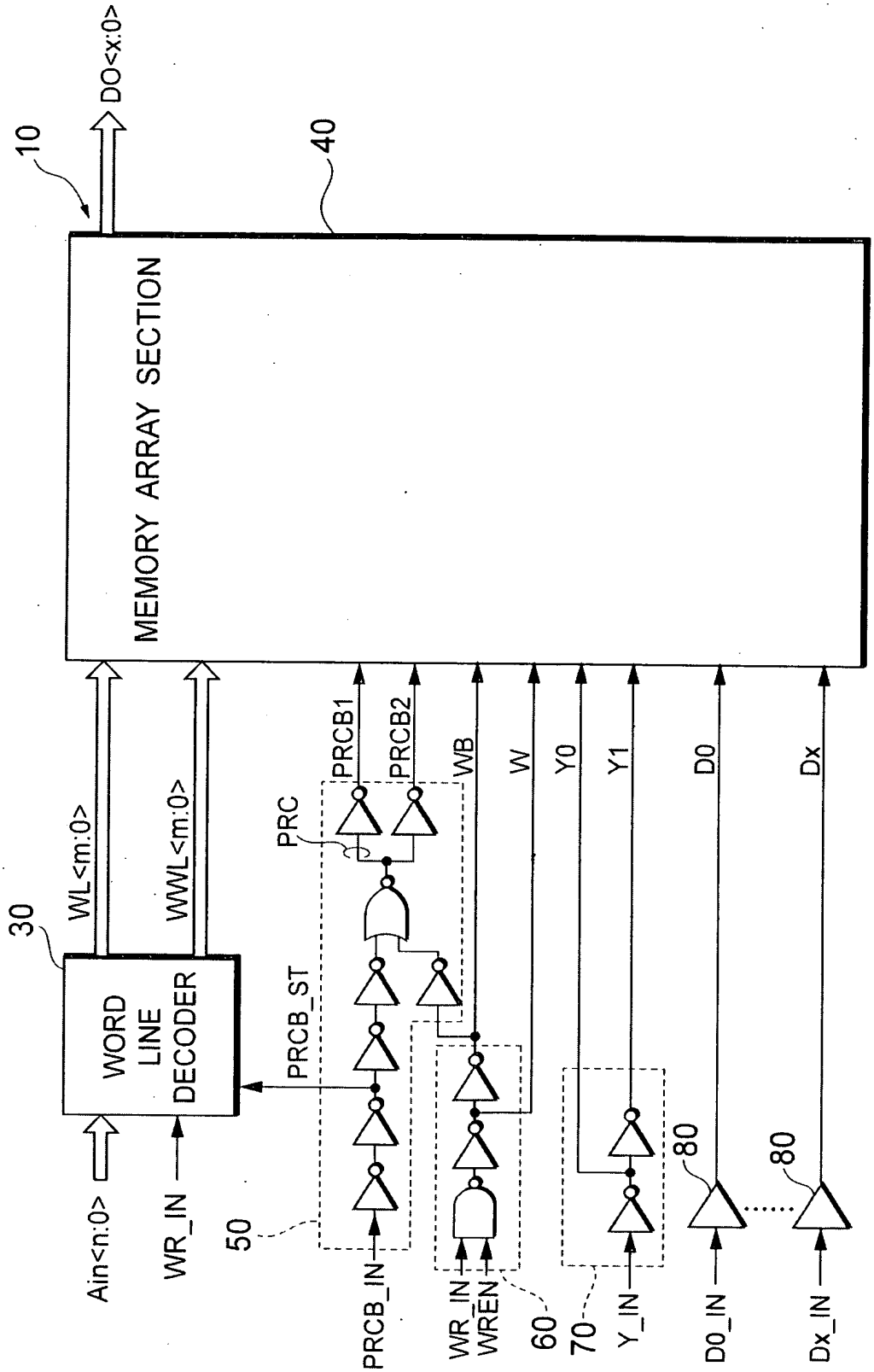
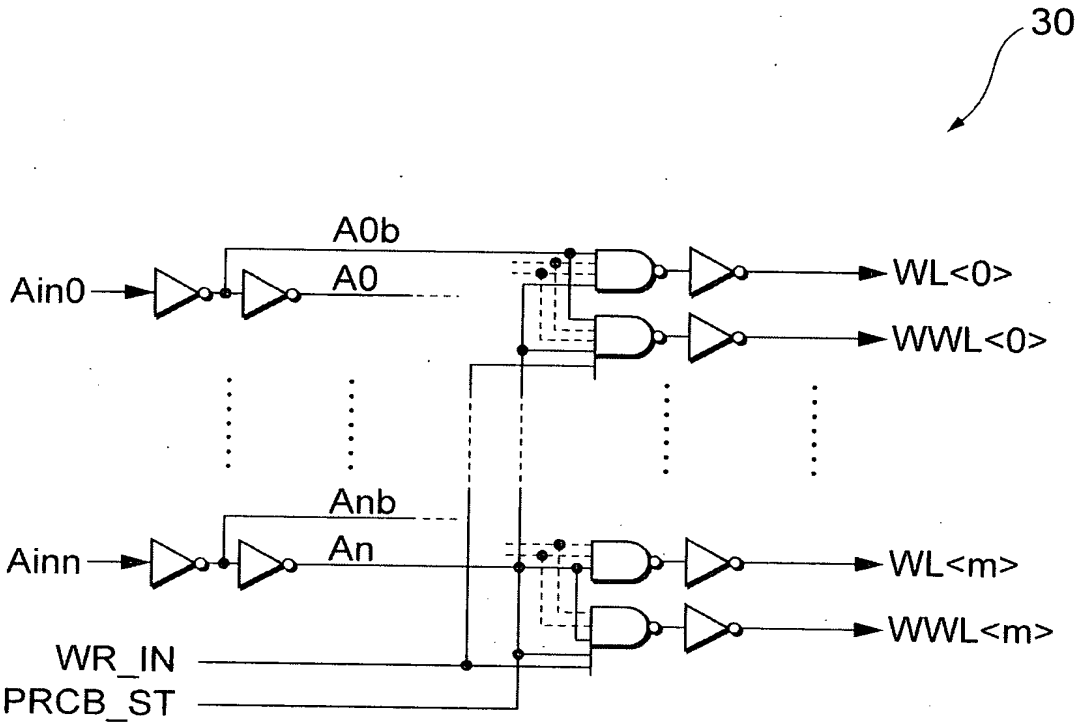

DO<x:0>
10
40
MEMORY ARRAY SECTION
WL<m:0>
WWL<m:0>
30
WORD LINE DECODER
Ain<n:0>
WR_IN
PRC
PRCB1
PRCB2
WB
W
Y0
Y1
D0
Dx
PRCB_ST
50
PRCB_IN
WR_IN
WREN
60
70
Y_IN
80
D0_IN
80
Dx_IN

*Fig.3*



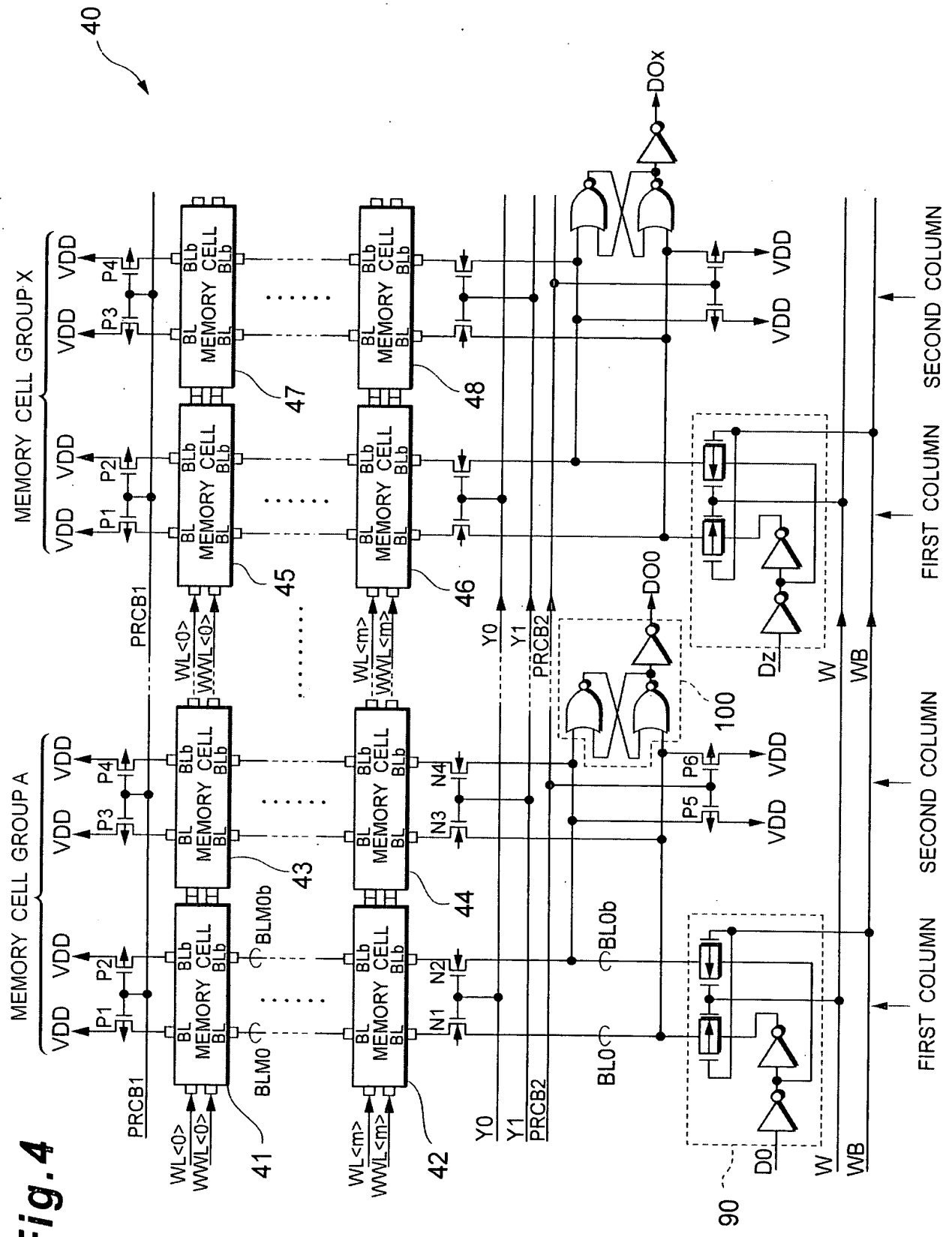
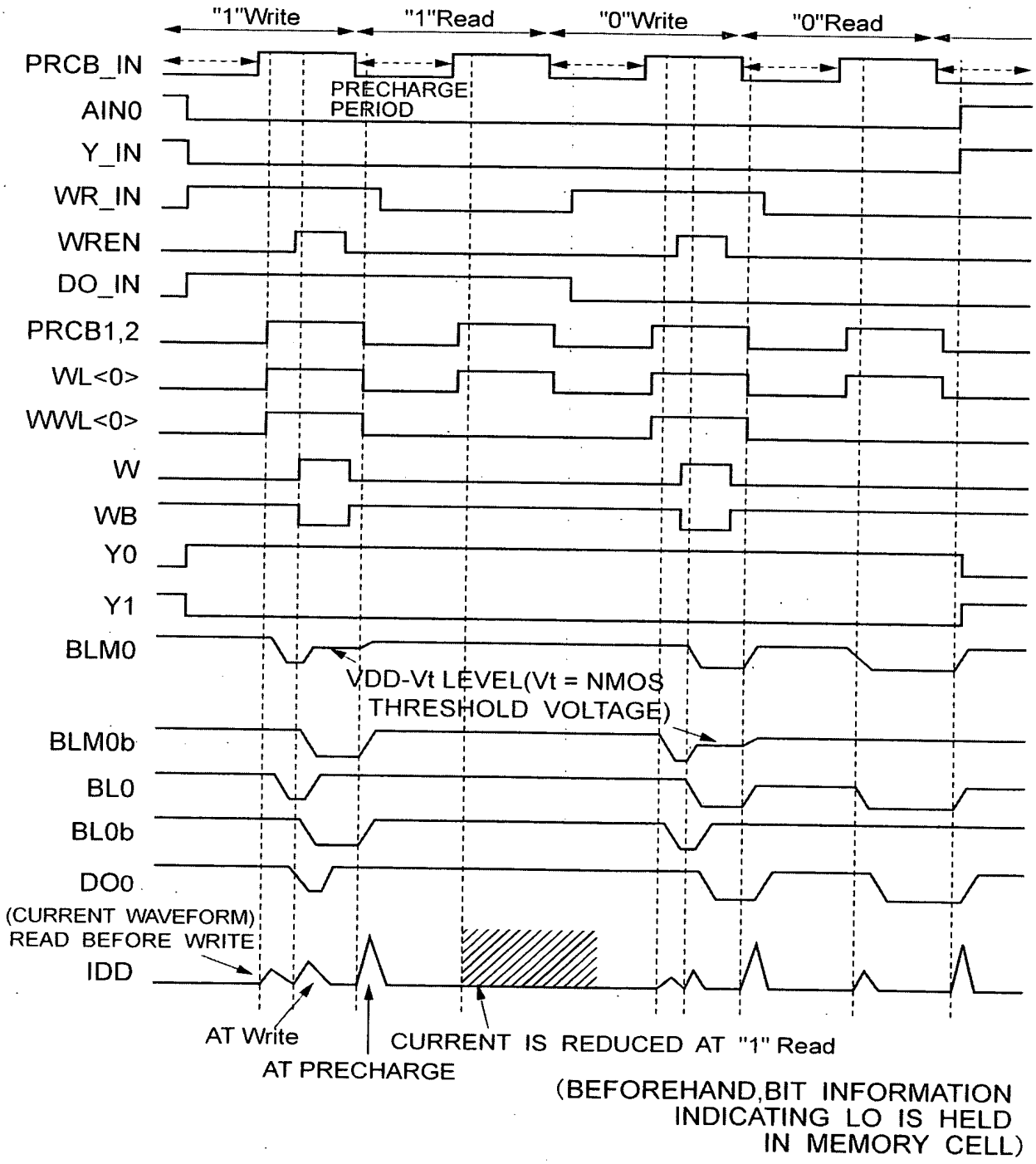

40
MEMORY CELL GROUP X
MEMORY CELL GROUP A
VDD
P1
P2
P3
P4
N1
N2
N3
N4
P5
P6
BL
BLb
MEMORY CELL
41
42
43
44
45
46
47
48
PRCB1
PRCB2
WL<0>
WWL<0>
WL<m>
WWL<m>
BLM0
BLM0b
BL0
BL0b
Y0
Y1
DOx
DO0
D0
Dz
W
WB
100
90
FIRST COLUMN
SECOND COLUMN

Fig. 4

# Fig.5


"1"Write
"1"Read
"0"Write
"0"Read
PRCB_IN
PRECHARGE PERIOD
AIN0
Y_IN
WR_IN
WREN
DO_IN
PRCB1,2
WL<0>
WWL<0>
W
WB
Y0
Y1
BLM0
VDD-Vt LEVEL(Vt = NMOS THRESHOLD VOLTAGE)
BLM0b
BL0
BL0b
DO0
(CURRENT WAVEFORM)
READ BEFORE WRITE
IDD
AT Write
AT PRECHARGE
CURRENT IS REDUCED AT "1" Read
(BEFOREHAND,BIT INFORMATION INDICATING LO IS HELD IN MEMORY CELL)

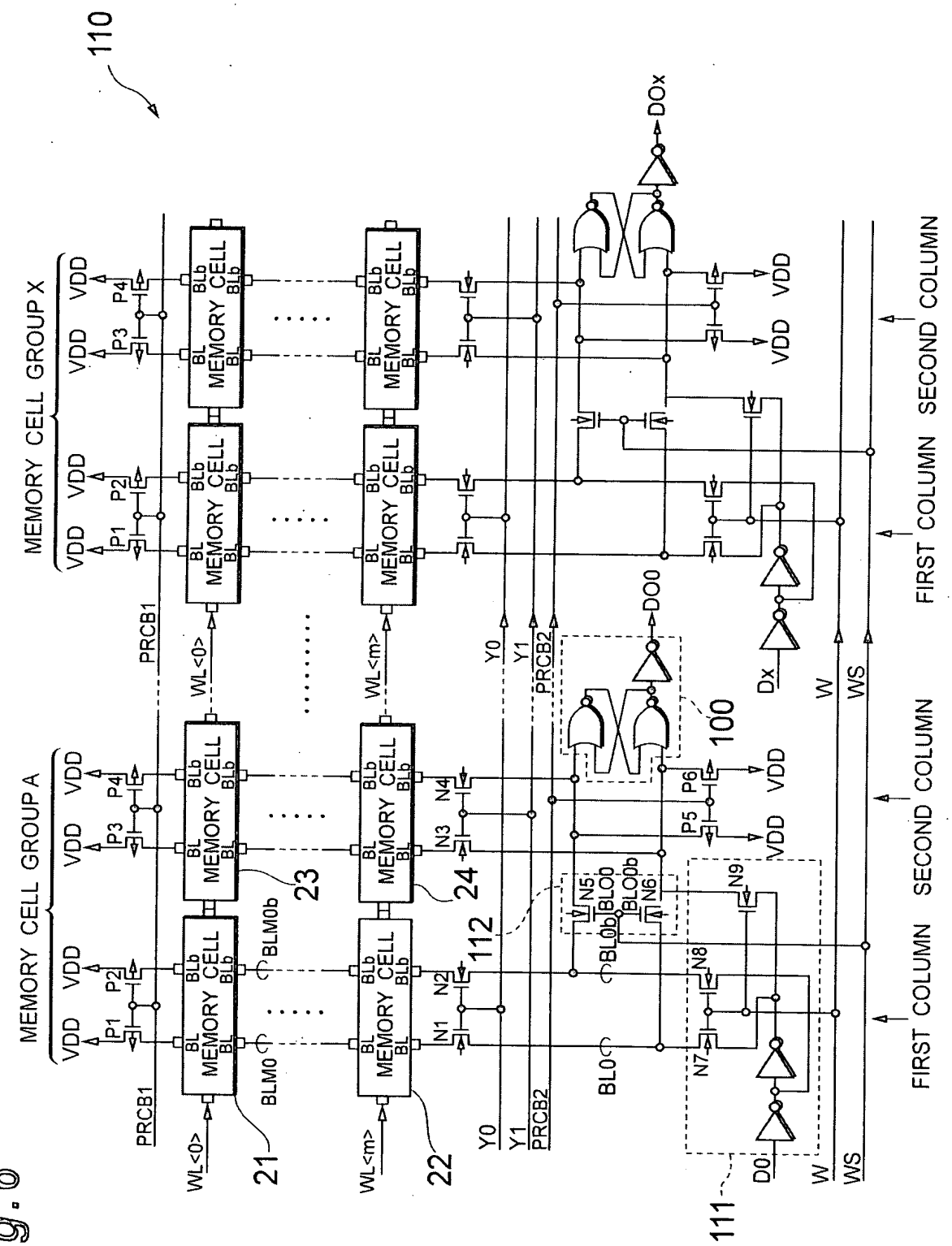

110
MEMORY CELL GROUP X
MEMORY CELL GROUP A
VDD
P1
P2
P3
P4
BL
BLb
MEMORY CELL
PRCB1
PRCB2
WL<0>
WL<m>
BLM0
BLM0b
21
22
23
24
112
100
111
Y0
Y1
BL0
BL0b
N1
N2
N3
N4
N5
N6
N7
N8
N9
P5
P6
DO0
DOx
Dx
D0
W
WS
FIRST COLUMN
SECOND COLUMN

Fig. 6

# Fig.7

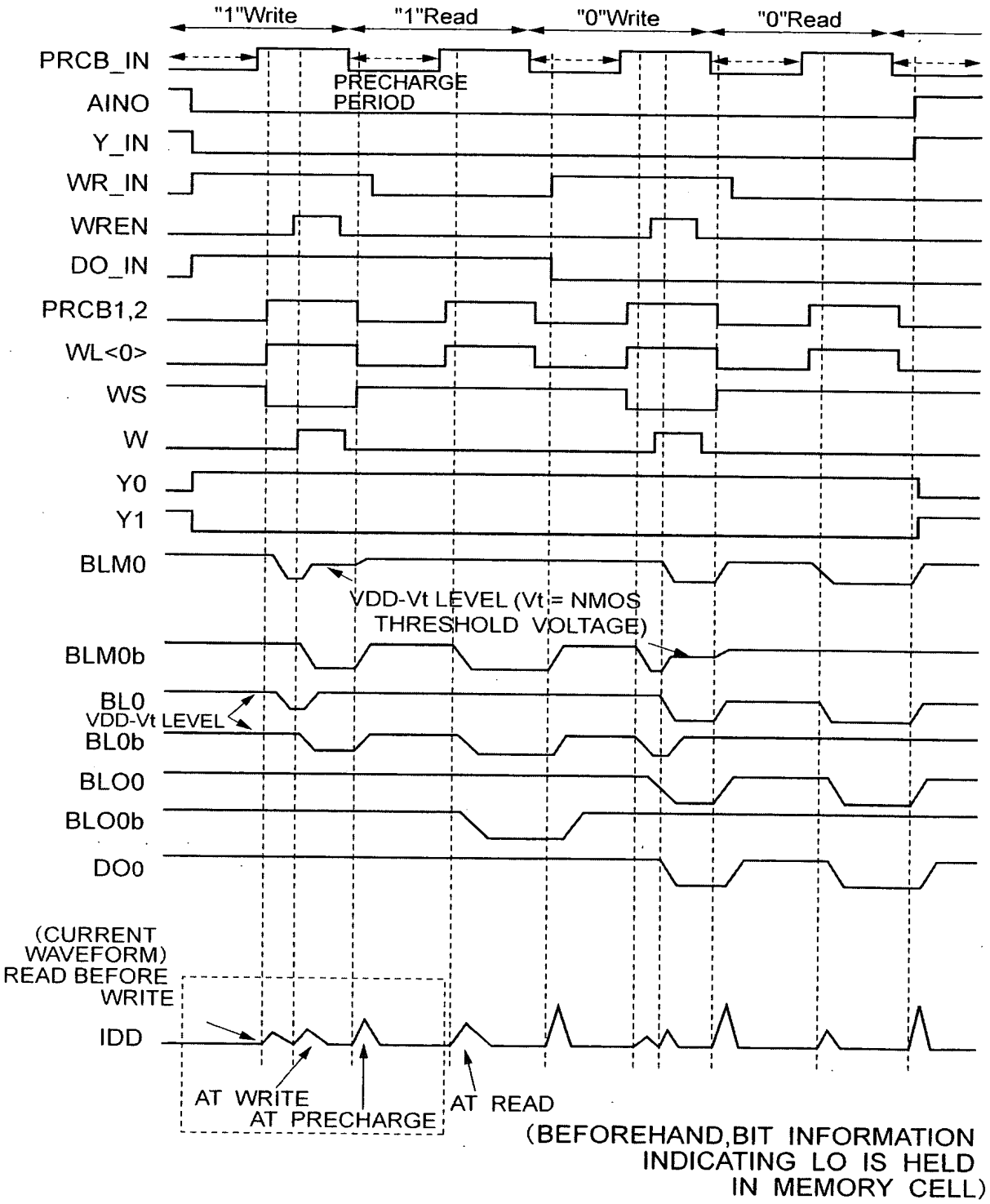

"1"Write
"1"Read
"0"Write
"0"Read
PRCB_IN
PRECHARGE PERIOD
AINO
Y_IN
WR_IN
WREN
DO_IN
PRCB1,2
WL<0>
WS
W
Y0
Y1
BLM0
VDD-Vt LEVEL (Vt = NMOS THRESHOLD VOLTAGE)
BLM0b
BL0
VDD-Vt LEVEL
BL0b
BLO0
BLO0b
DO0
(CURRENT WAVEFORM) READ BEFORE WRITE
IDD
AT WRITE
AT PRECHARGE
AT READ
(BEFOREHAND,BIT INFORMATION INDICATING LO IS HELD IN MEMORY CELL)

*Fig.8*

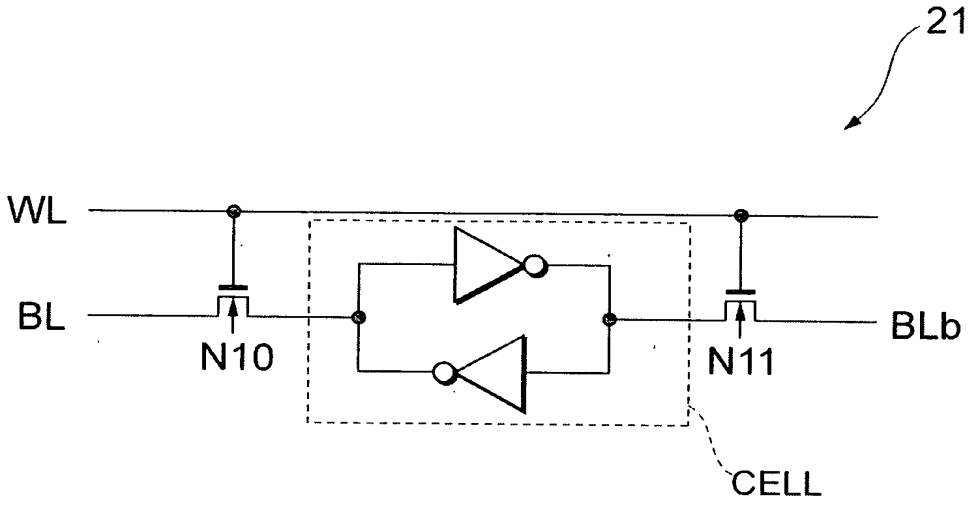



*Fig.9*

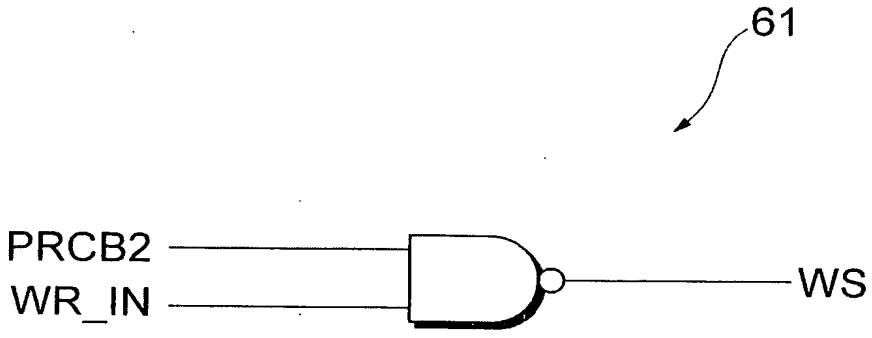


Fig.10

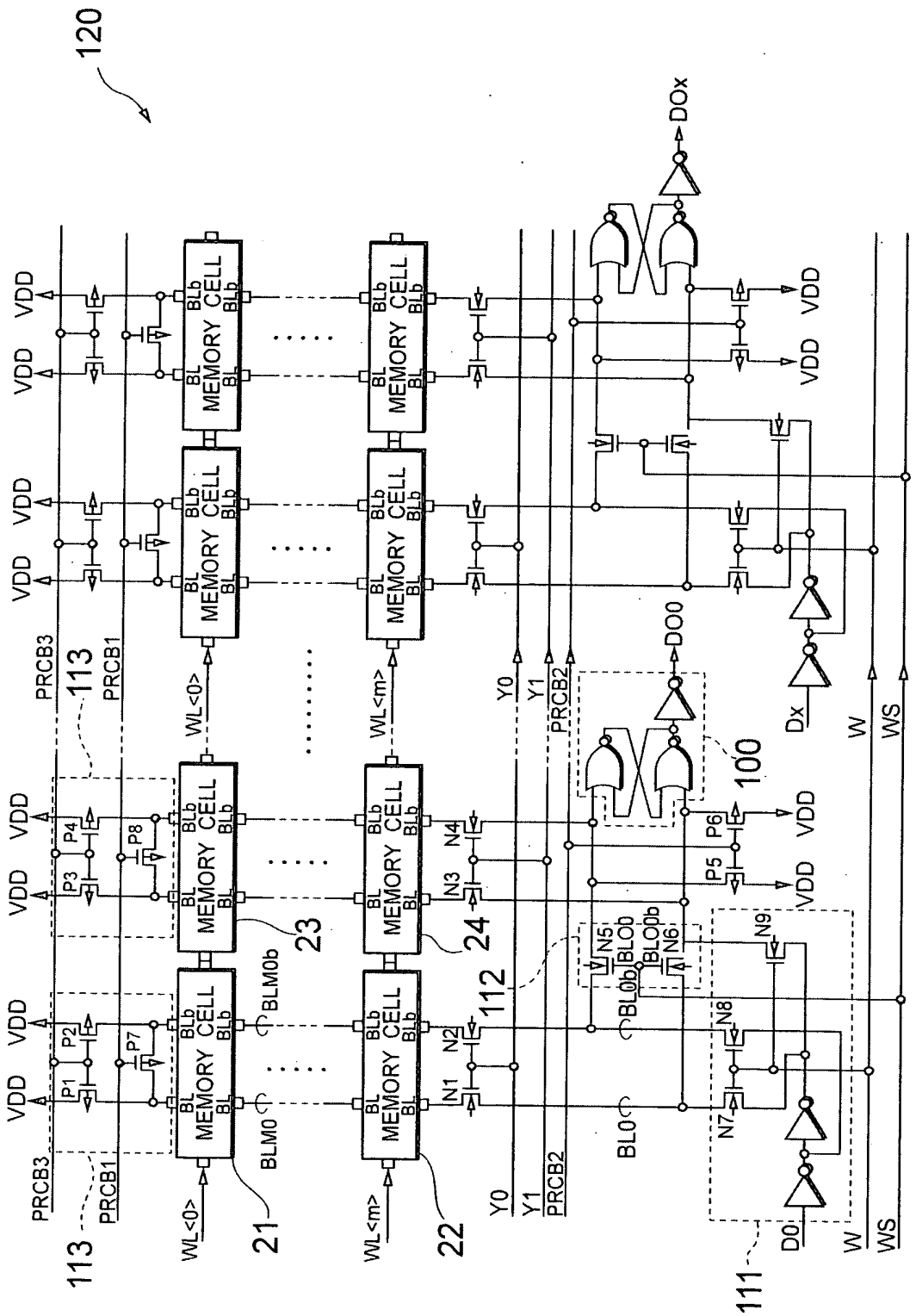

120
DOx
DO0
Dx
D0
VDD
PRCB3
PRCB1
PRCB2
113
111
112
100
WL<0>
WL<m>
BLM0
BLM0b
BL0
BL0b
21
22
23
24
Y0
Y1
W
WS
MEMORY CELL
BL
BLb
P1
P2
P3
P4
P5
P6
P7
P8
N1
N2
N3
N4
N5
N6
N7
N8
N9

Fig.11

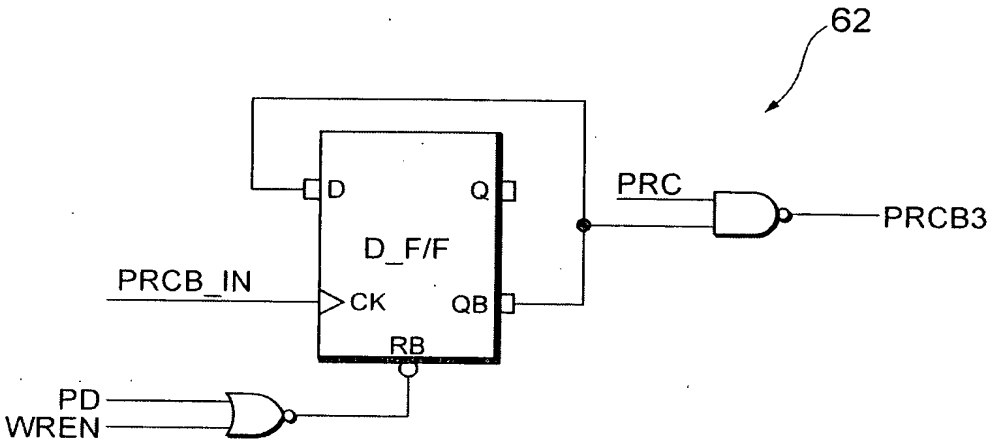
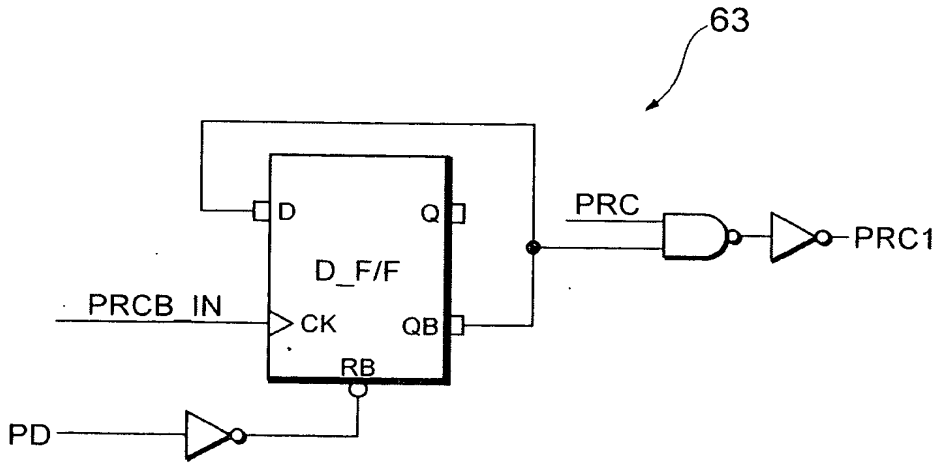

62
D
Q
D_F/F
PRC
PRCB3
PRCB_IN
CK
QB
RB
PD
WREN

Fig.14


63
D
Q
D_F/F
PRC
PRC1
PRCB_IN
CK
QB
RB
PD

# Fig.12(a)

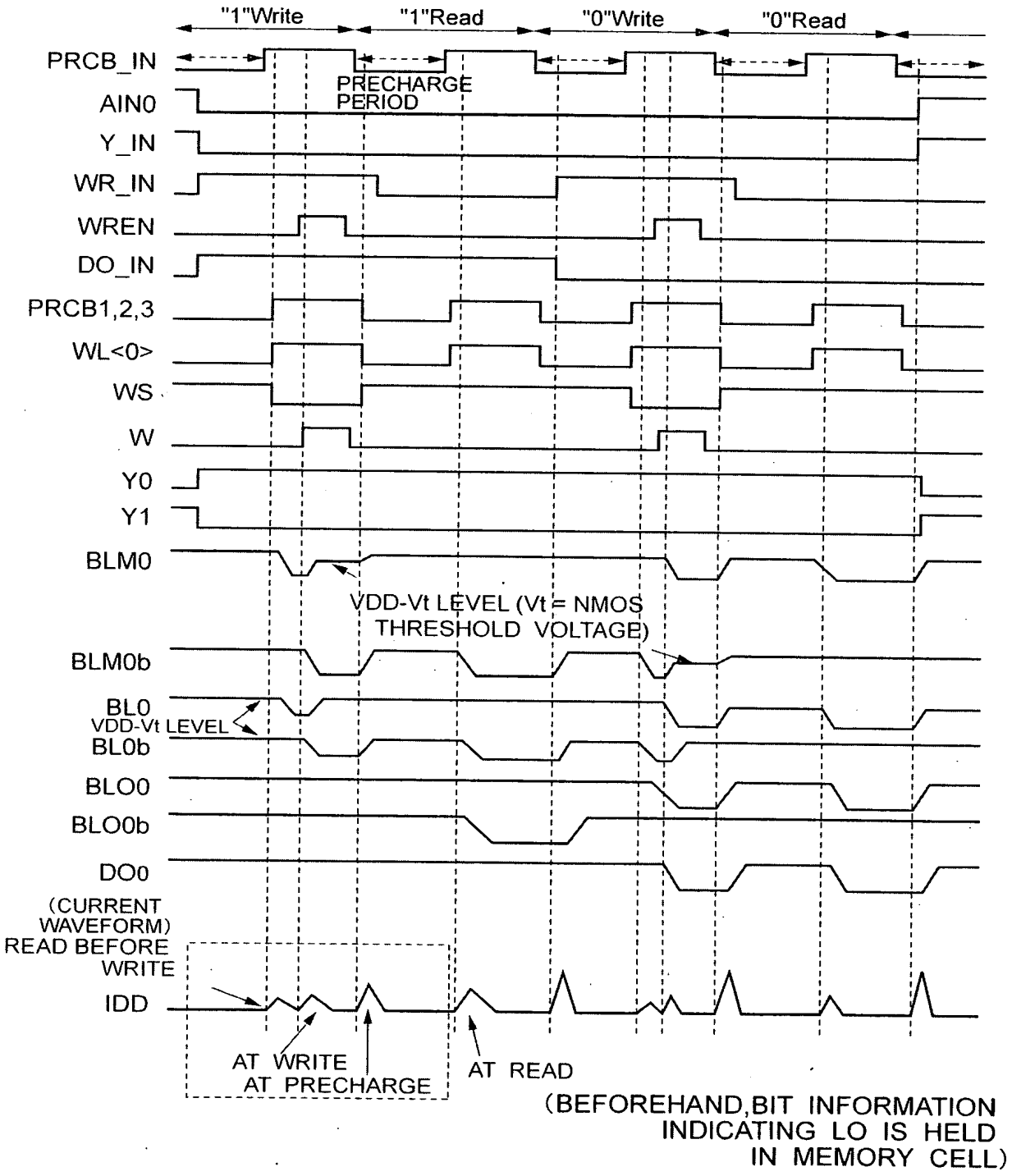

"1"Write
"1"Read
"0"Write
"0"Read
PRCB_IN
PRECHARGE PERIOD
AIN0
Y_IN
WR_IN
WREN
DO_IN
PRCB1,2,3
WL<0>
WS
W
Y0
Y1
BLM0
VDD-Vt LEVEL (Vt = NMOS THRESHOLD VOLTAGE)
BLM0b
BL0
VDD-Vt LEVEL
BL0b
BLO0
BLO0b
DO0
(CURRENT WAVEFORM) READ BEFORE WRITE
IDD
AT WRITE AT PRECHARGE
AT READ
(BEFOREHAND,BIT INFORMATION INDICATING LO IS HELD IN MEMORY CELL)

Fig.12(b)

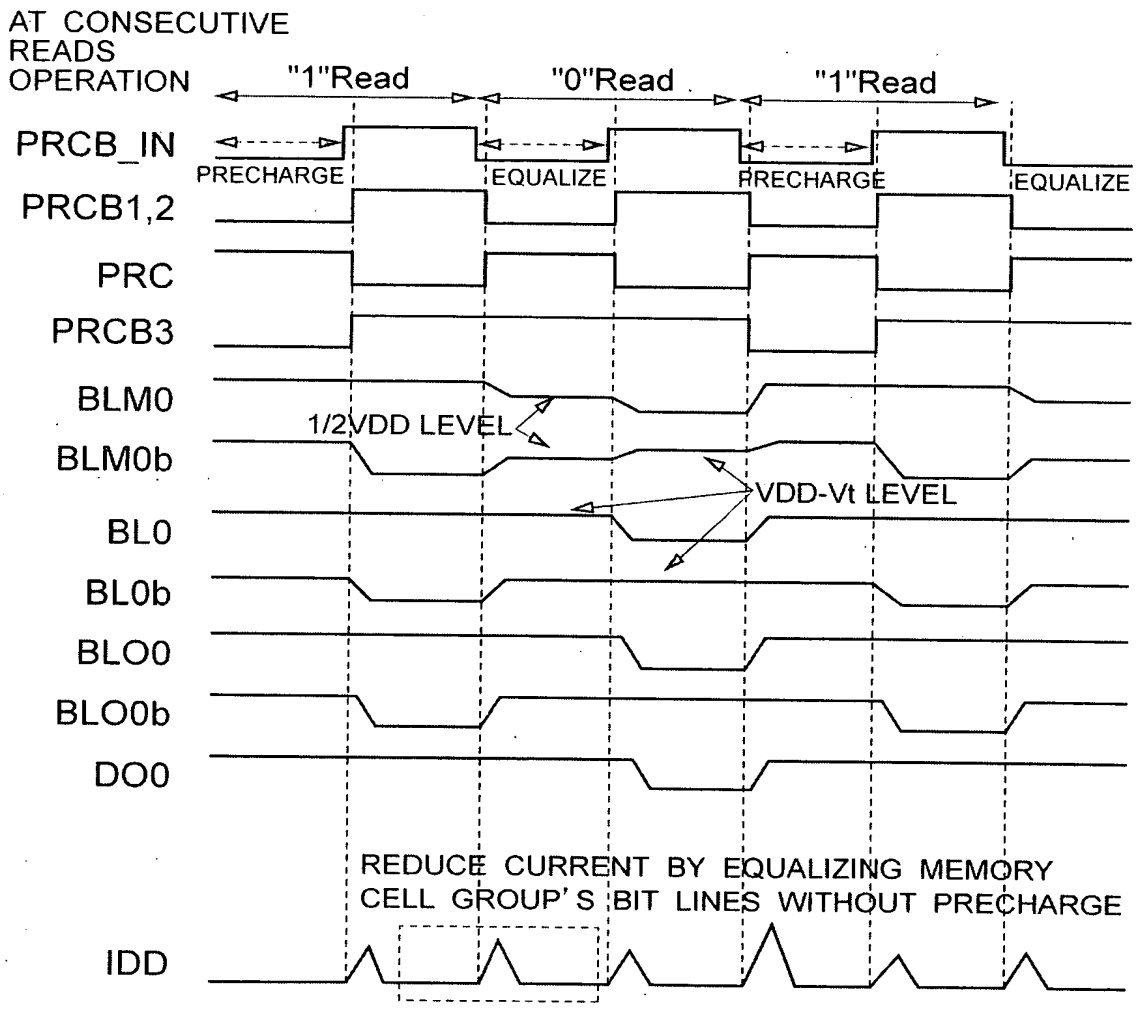

AT CONSECUTIVE READS OPERATION
"1"Read
"0"Read
"1"Read
PRCB_IN
PRECHARGE
EQUALIZE
PRECHARGE
EQUALIZE
PRCB1,2
PRC
PRCB3
BLM0
1/2VDD LEVEL
BLM0b
VDD-Vt LEVEL
BL0
BL0b
BLO0
BLO0b
DO0
REDUCE CURRENT BY EQUALIZING MEMORY CELL GROUP'S BIT LINES WITHOUT PRECHARGE
IDD

Fig. 13

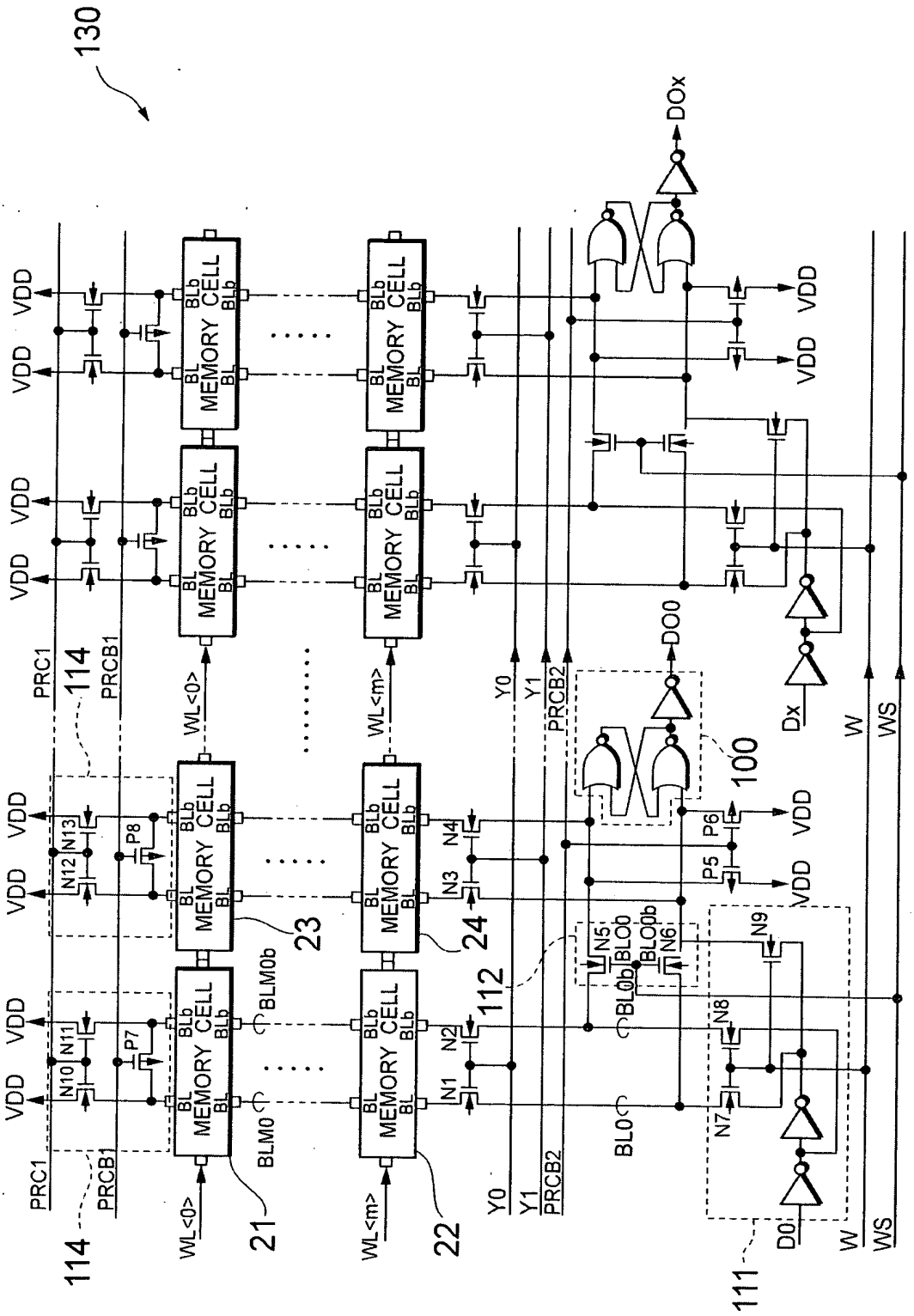
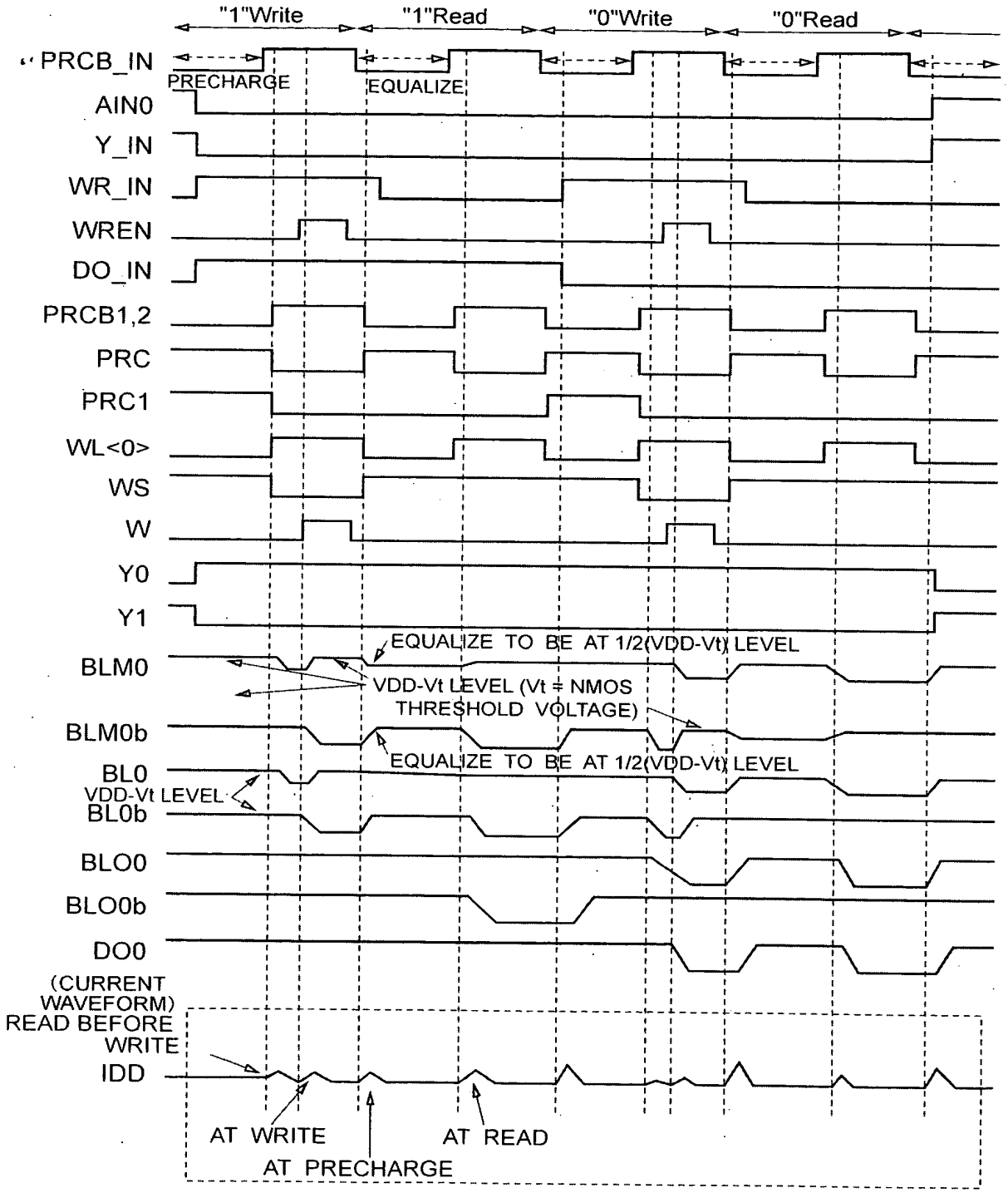

130
DOx
VDD
MEMORY CELL
BL
BLb
PRC1
PRCB1
114
WL<0>
WL<m>
BLM0
BLM0b
21
22
23
24
112
100
DO0
Dx
Y0
Y1
PRCB2
P5
P6
P7
P8
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
N12
N13
BL0
BL0b
DO
W
WS
111

Fig.15




(BEFOREHAND,BIT INFORMATION INDICATING LO IS HELD IN MEMORY CELL)